Docket No. 52352-757 (F0173)

PASSIVATION OF NITRIDE SPACER

Field of Invention

The invention pertains to passivating a silicon nitride spacer to prevent silicide bridging between the gate electrode and the source and drain regions.

Background of the Invention

Fig. 1 shows a typical prior art MOSFET device 10 comprising a semiconductor substrate 11, field oxide (FOX) regions 12, source and drain regions 13 and 14, and a gate electrode 15. The substrate 11 consists of a P-doped single crystalline silicon to form a P type substrate. The thick field oxide (FOX) regions 12 are formed on either side of the source and drain regions 13 and 14 for isolation purposes. The gate electrode is formed on the surface of semiconductor substrate between the source and drain regions. The gate electrode typically includes a thin silicon oxide layer 16 and a polysilicon layer 17. Silicon dioxide spacers 18 formed on the sidewalls of the gate electrode. Refractory metal silicide contacts 19 and 20 are formed typically on the surface of drain and source regions 13 and 14 on the horizontal surface of substrate 11 and on the horizontal top surface 21 of the gate electrode by a process known as a self-aligned silicide or salicide process. The silicides result from the thermal reaction of the metal and silicon in regions 13 and 14 and polysilicon layer 17.

While the sidewall spacers are intended to prevent bridging of the gate silicide region with either the source or drain silicide regions, as device geometries become smaller, bridging between the silicide formed on the top surface 21 and the metal silicide contacts 19 and 20 has again become a serious problem. It is known that native oxide or oxide residues from the anisotropic etching to form the silicon oxide spacers will form on the exposed top surface of the polysilicon gate as well as on the top surfaces of the source and drain regions. These oxides must be removed to allow the subsequent metal silicide formation to be successful because the oxides will prevent the reaction between the metal and the exposed silicon surfaces during the annealing step. In order to remove the oxides, the surfaces are typically treated with 1 vol. % HF solution prior to deposition of the metal. However, while hydrofluoric acid etches the native oxide, it also etches the silicon oxide spacers 18 causing significant thinning and exposing the surface of the polysilicon 17 in the gate structure resulting in a

metal silicide being formed during the salicide process to cause bridging to occur on the sides of the polysilicon gate.

A solution to the problem is disclosed in U.S. Patent Nos. 5,747,373 and 5,851,890 wherein a double insulator spacer is used to prevent the metal silicide bridging phenomena. Specifically, the spacer comprises two layers, a first layer comprising silicon oxide that is formed on the sides of the polysilicon gate and a second layer comprising silicon nitride which is formed on the first layer. The double layer prevents the oxide layer from being etched because it is not affected by the HF etchant.

However, the silicon nitride includes with dangling silicon bonds that can react with the metal during the salicide process. Most notably this occurs with nickel. These bonds form a thin nickel silicide layer over the spacer. This thin layer leads to bridging between the gate electrode and the source and drain regions of the transistor which can result in an increase in transistor resistance.

It has been discovered that by coating the nitride layer with a thin layer of silicon oxide prior to the etching and the salicide process, the bridging problem is significantly reduced, if not eliminated.

Summary of the Invention

The object of this invention is to provide passivate silicon nitride spacers by coating the spacers with a thin coating of silicon oxide to avoid silicidation bridging. To accomplish the object described above according to the present invention, there is provided a method for which comprises the steps of covering the entire surface of an semiconductor substrate including source and drain regions, a gate electrode with a thin layer of silicon oxide, etching the top surface of the gate electrode and the top surfaces of the source and drain regions just prior to depositing the metal in the silcitation process. The other objects and characteristics of the present invention will become apparent from the further disclosure of the invention which is given hereinafter with reference to the accompanying drawing.

Brief Description of the Drawing

A more complete appreciation of the invention and many of the attendant advantages thereof will be readily obtained as the same become better understood by reference to the following detailed description when considered in connection with the accompanying drawing.

Fig. 1 is a sectional side view showing a prior art structure illustrating an integrated circuit structure on a silicon substrate with silicon dioxide spacers on the sidewalls of a polysilicon gate electrode.

Figs. 2A-2E schematically illustrate, in cross-sectional style, the key stages for fabricating a MOSFET device with silicon nitride spacers featuring a thin silicon oxide layer on the spacers to passivate the nitride during the salicide process.

Detailed Description of the Invention

This invention relates to a method and a semiconductor device prepared therefrom for passivation of a silicon nitride layer to prevent bridging between the gate and electrode and the source and drain regions of the transistor in a semiconductor device.

Fig. 2A is a cross-sectional view of the first stage of the process. A semiconductor substrate 11 is shown having isolation regions 12. The semiconductor substrate can be silicon or or an silicon on insulator (SOI) structure. The substrate 11 can be an N-type or P-type silicon. For illustrative purposes only, Fig. 2A shows semiconductor substrate as a single crystalline silicon is doped with a P-type dopant.

The isolation regions 12 may be shallow trench isolation (STI) regions or field oxide (FOX) regions that can be formed using any know localized oxidation of silicon (LOCOS) isolation methods. For example, thick field oxide (FOX) regions 12 can be formed by thermal oxidation in an oxygen-steam ambient at a temperature between 850° to 1050° C. The thickness of the regions is from about 4000 to about 6000 Å. Oxidation is prevented in the region between the FOX regions by using a patterned, oxidation resistant mask that is removed after the oxidation process is completed.

The gate electrode 15 comprises a dielectric layer 16 and a gate conductor layer 17. The gate dielectric layer 16 is formed on upper surface of substrate 11 between isolation regions 12. The gate electrode dielectric layer is typically silicon oxide, but it can also be silicon oxynitride or a high-K dielectric such as tantalum pentoxide (Ta_2O_5). The layer can also be a composite layer of silicon oxide and silicon nitride. The thickness of the gate dielectric is from about 20 to about 100 Å. The gate dielectric layer can be formed by using conventional chemical vapor deposition (CVD) techniques.

The gate conductor layer 17 is formed over the gate dielectric layer 16. The gate conductor is a polysilicon material and is about 400 to about 1000 Å thick. The polysilicon material is typically a mixture of polysilicon and amorphous silicion. Once formed, the gate dielectric and conductor layer is patterned to form a gate structure by using well known photolithographic and etching techniques. The thickness of the total gate electrode is between 420 Å and 1100 Å. The gate electrode is formed by providing a layer of silicon dioxide as the gate insulator layer by thermally growing the oxide in an oxygen-steam ambient at a temperature between 850° to 1050° C. to a thickness between about 50 and about 200Å. Next, a polysilicon layer is deposited on the gate insulator by any conventional process such as a low pressure chemical vapor deposition process at a temperature between 600° to 800° C. The thickness of the gate insulator is from about 500 Å to about 5000Å. The polysilicon layer can be doped using conventional techniques and conventional photolithographic and reactive etching procedures to create the polycrystalline gate structure. The width of the polycrystalline gate structure is between about 50 nm and about 1 μm.

Fig. 2B shows forming the source and drains regions 13 and 14 adjacent to the opposite sides of the gate electrode. The formation of the source and drain regions can be accomplished by any known methods such as by the conventional ion implantation of phosphous or arsenic. Nothwithstanding the methods, for illustrative purposes only, Fig. 2B shows semiconductor substrate as a P-type silicon and and the source and drain regions as doped N-type. Alternatively, but not shown, the semiconductor substrate could be an N-type and the source and drain regions could be P-type.

Silicon nitrde sidewall spacers 18 are used during the formation of the source and drain regions 13 and 14. The spacers 18 are formed by depositing a blanket layer of silicon nitride (not shown) and anisotropically etching the nitride layer to form spacers 18. The anisotropic etch method is selected because it will remove the nitride from the upper surface of the gate electrode and the surface of the semiconductor substrate, but not the nitride on the side walls of the gate electrode. The average typical thickness for each spacer is from about 50 to about 500Å.

In Fig. 2C, a thin silicon oxide layer 23 of is formed on the semiconductor substrate including the gate electrode, the spacers, the source and drain regions and the isolation regions. The thickness of

the layer is from about 20 Å to about 100 Å. The silicon oxide layer is formed by treating the substrate in a mixture of sulfuric acid and hydrogen peroxide at a temperature of about 300° C. The thin silicon oxide layer is removed from the surface of the source and drain regions and the top surface of the gate electrode to form the device shown in Fig. 2D

Fig. 2E shows a blanket layer 24 of nickel deposited on the top surface semiconductor substrate including the gate electrode, spacer, the source and drain regions and the isolation regions. The nickel layer is deposited by using a PVD process such as DC sputtering. The thickness of the refractory metal deposited in this step depends upon several factors, including, *inter alia*, the particular selected metal, its Si consumption ratio, and desired thickness (hence resistivity) of the resultant refractory metal silicide. The conversion of Ni to NiSi may be accomplished by means of a one-step thermal process, typically RTA performed at temperatures of from about 350 to about 750°C, for example, in a nitrogen (N_2)-containing inert atmosphere at 550°C for about 40 sec. The formation of NiSi commences at about 250°C, when the Ni layer reacts with silicon to form Ni_2Si. With increase in reaction time or temperature to above about 300°C, the Ni_2Si undergoes further reaction with silicon in the source and drain regions and with the polysilicon material in the gate conductor to form NiSi layers 25, 26 and 27, respectively, as shown in Fig. 2F. Because of the thin silicon oxide on the spacers, no nickel silicide is formed on the nitride spacer.

Unreacted nickel must be removed from areas where silicide does not form to produce the device shown in Fig. 2G. This is accomplished by using an anisotropic sputter etching or by etching with a 2:1 H_2SO_4/H_2O_2 mixture at a temperature of about 100°C.

The foregoing is considered as illustrative only of the principles of the invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation shown and described, and accordingly, all suitable modifications and equivalence thereof may be resorted to, falling within the scope of the invention claimed